REMARKS

Claims 1-13 are pending in this application. The Examiner rejects all of the pending claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Baker et al. (Baker). Applicant respectfully traverses the Examiner's rejection as follows.

As noted in Applicant's Response filed March 18, 2004, Applicant's invention is in the field of multitasking digital signal processors, and provides a real time control system comprising unique combinations of features, including *inter alia*:

> a ready queue including a ready queue link, the ready queue link comprising
>
> a first information indicating a first task control block for a sequentially first task among tasks in the digital signal processor, and a second task control block for a sequentially last task among the tasks in the digital signal processor,
>
> a priority link group of priority links, a number of the priority links being equal to a number of priority levels of the tasks in the digital signal processor, and
>
> a second information indicating a third task control block for a sequentially first task among tasks having same priority among the tasks in the digital signal processor, and a fourth task control block for a sequentially last task among the tasks having same priority; and
>
> an operating system for setting the first and second information according to conditions of tasks for the digital signal processor, and controlling switching between the tasks of the ready queue. (Applicant's independent claim 1).

In particular, one of the features of Applicant's claimed invention is a ready queue link which comprises, *inter alia*, "a first information indicating ... a second task control block for a **sequentially last task among the tasks** in the digital signal processor," and "a second

information indicating ... a fourth task control block for **a sequentially last task among the tasks having same priority**" (Applicant's claim 1, emphasis added).

As explained in great detail in Applicant's Response filed March 18, 2004, nowhere does Baker disclose, teach or suggest that its TMS utility obtains, stores or uses information indicative of a task control block for a sequentially last task among the tasks in its DSP. Likewise, nowhere does Baker disclose, teach or suggest that its TMS utility, or its QMS utility, obtains, stores or uses information indicative of a task control block for a sequentially last task among the tasks having the same priority in its DSP. Thus, Baker is incapable of teaching or suggesting a ready queue link comprising, *inter alia*, information indicating a task control block for a **sequentially last task among the tasks** in the digital signal processor, and information indicating a task control block for **a sequentially last task among the tasks having same priority**, as explicitly recited in Applicant's independent claim 1.

In the reply to Applicant's argument presented in the Response filed March 18, 2004, the Examiner cites Baker at "Fig. 6, col. 9 lines 47-65, col. 10, lines 61-65, col. 11 lines 22-32, col. 12 lines 64-68, col. 13, lines 7-14 and col. 16 lines 47-58" (see final Office Action, page 8, paragraph 19). The portions of Baker cited by the Examiner are reproduced below, in their entirety, for reference:

> With reference to FIG. 6, ROM 110 of instruction store 106 generally holds the instructions, programs, code for functions and tasks that are used by or in connection with other tasks or programs tailored to or defining specific tasks for functions of each different ASH. ROM 110 includes a real-time operating system (RTOS) 300, a power-on diagnostics program 302, and various communications protocols including asynchronous 304, SDLC/HDLC 306, binary synchronous 308, and different modem protocols 310. A checksum program 312 is also stored

in ROM 110. Instruction store RAM 108 contains the code for different tasks which code is loaded therein by the PC or host. "PC" is used herein as a relative term to refer to that part of the personal computer system outside of DSPSS 64.

Data store 104 stores mapped I/O control registers 318, shadow registers, port I/O, set up registers, etc. 320, RTOS data area 322, intertask communication buffers 324, task defined buffers, tables, etc. 326, and task control blocks (TCBs) 328.

(Id., col. 9, lines 47-65.)

In case the inserted task has the same COUNT as a task which is already in the queue, it will get inserted after it. Thus, tasks which have the same COUNT will be executed by executor 356 in the same order in which they are linked to TMS.

(Id., col. 10, lines 61-65.)

When QMS reaches the head of the ordered execution queue and commences execution, it starts to load its linked real-time tasks into execution serially, according to the order in which they are linked. It is the same order as if they had been inserted into the execution queue by the TMS task directly. When the list is exhausted, i.e., the next task is QMS itself (circular QMS list), QMS terminates as any RTOS task by returning to the background executor according to the BGXRTN contents.

(Id., col. 11, lines 22-32.)

Each task has a Task Control Block (TCB) stored at a predetermined location in data store 104. The TCB provides system information about the task and a limited number of user links to other tasks' TCBs.

(Id., col. 12, lines 64-68.)

Execution queue 358 contains both real-time and non-real-time tasks, ordered according to the task's relative priority. Priority is determined by the time to the next execution instant. Those tasks that have the least amount of time prior to the next execution instant will gain the highest priority on the queue. Non-real-time

> tasks which do not have a definite time frame in which they must complete their execution, are placed at the end of the execution queue.
>
> (Id., col. 13, lines 6-15.)

> a plurality of task control blocks (TCBs) stored in said data store, there being a different TCB associated with each task, each TCB containing a plurality of fields for storing, for the associated task, 1) a frame defining a scheduling period between successive scheduling of said associated task, 2) a scheduling count defining when the associated task is to be next scheduled, 3) DSP information for restoring said DSP when an interrupted task is next executed, and 4) an instruction address at which to begin initial execution of said associated task
>
> (Id., col. 16, lines 47-48.)

Upon close review of Baker, one skilled in the art of control systems for digital signal processors would readily appreciate that, nowhere does Baker disclose, or even remotely suggest, a ready queue link comprising, *inter alia*, information indicating a task control block for a **sequentially last task among the tasks** in the digital signal processor, and information indicating a task control block for **a sequentially last task among the tasks having same priority**, as recited in Applicant's independent claim 1.

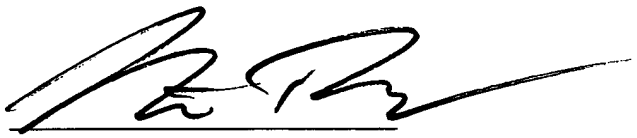
Therefore, Applicant's independent claim 1, as well as its dependent claims 2-13 (which incorporate all the novel and unobvious features of their base claim), would not have been obvious from Baker at least for this reason.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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